Experiment #8

Serial Adder

Objectives:

- To investigate the operation of a gated SR latch with asynchronous preset and clear inputs.
- To investigate the operation of a serial adder which uses the above device.

Discussion:

One implementation of a gated SR latch with asynchronous preset (PR) and clear (CLR) inputs is shown in *Figure 8-1* and its associated symbol is shown in *Figure 8-2*.

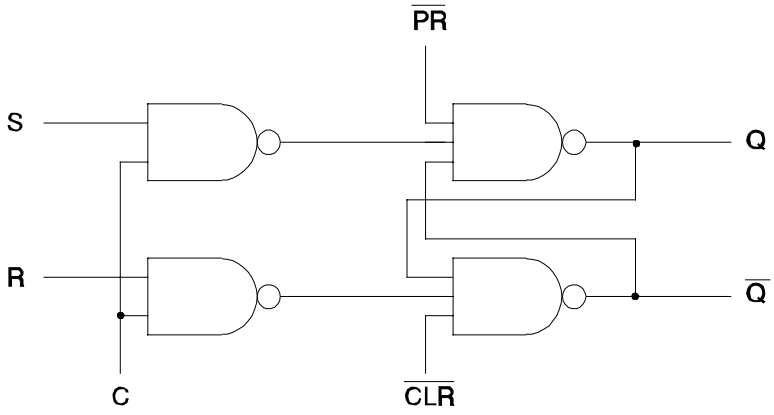

Figure 8-1: SR Latch Logic Diagram

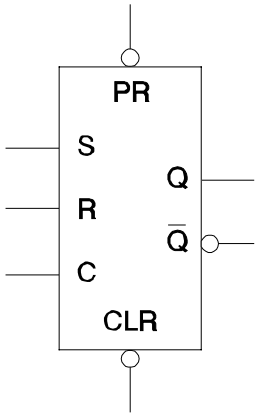

Figure 8-2: SR Latch Symbol

The Set and Reset inputs are synchronous inputs. The C line "enables" these inputs to affect the change of state of the device. The synchronous operation of this device is a "latching" operation. The outputs Q and $\overline{Q}$ will react to the S and R inputs during the time that C=1.

The PReset and CLeaR inputs are asynchronous inputs and are analogous to the Set and Reset inputs of the synchronous case. They are used, typically, to initialize a device to a 1 state or to a 0 state respectively. They are asynchronous inputs because the storage operation does not require the synchronizing signal C to be a "1". They are active-low inputs.

Another type of memory device is the D flip-flop. This type of memory device has one Data input line, the D input line. The level on the input line is stored in the device when the control line changes from inactive to active. Thus it is a "leading edge" or edge triggered device. The term flip-flop is used to describe this type of control.

The SR latch can be converted to a D latch by tying the input to the S line and the complement of the input to the R line (see *Figure 8-3*). The operation of the D latch can approach the operation of a D flip-flop by inserting the "pulse shortening" circuit before the clock line.

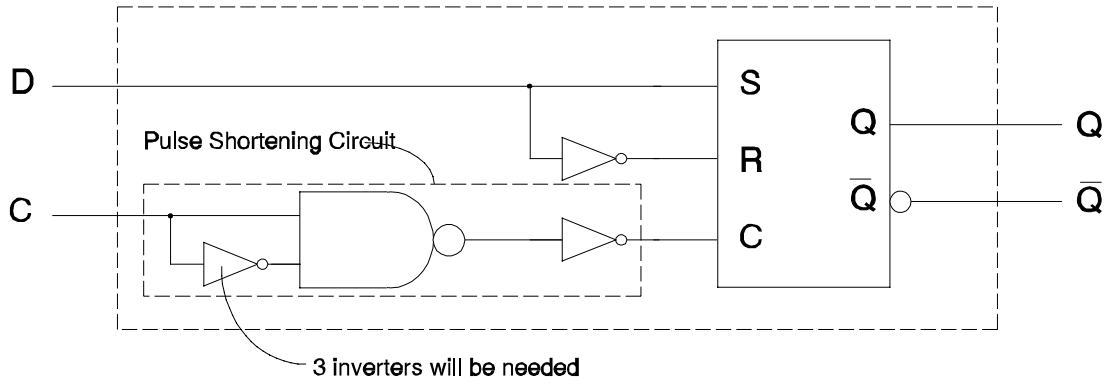

Figure 8-3: D Latch With Pulse Shortening Circuit

Binary adder circuits are presented in section 20.2 of the Roth text. Laboratory #4 addressed the design of a parallel adder. An alternative for binary addition is a serial scheme as shown in *Figure 8-4*. In this scheme, time is traded for space (or hardware). One full adder and one D flip flop is used for any length addition. Inputs X_i and Y_i are applied at time t_i; and S_i and CO_i are generated. The CO_i is stored in the D flip flop. If the inputs are applied at regular intervals $\Delta t = t_{i+1} - t_i$, then the time required to perform the addition of two n-bit numbers is $n\Delta t$. This is typically longer than the propagation delay associated with the parallel (addition) scheme of laboratory #4.

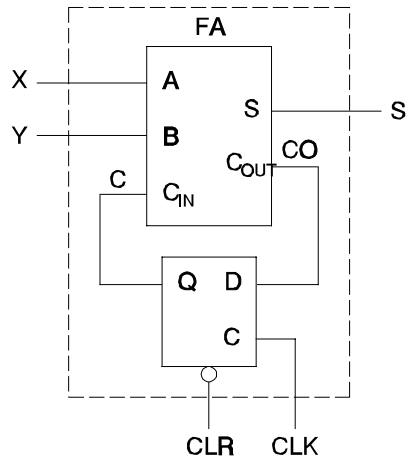

Figure 8-4: Serial Adder

Design Problem:

You are to design a serial adder with the following specifications. The data inputs are X and Y; the data output is S. The control inputs are CLK and CLR. The CLK will accept any pulse length and the CLR line will cause the internal state to be set to "0". Signals C and CO must be available for analysis.

Pre-Lab Assignment:

1) Design a logic schematic for a solution to the above design problem using *NAND*, *XOR*, and Inverter gates.
2) Construct a timing diagram for the "pulse shortening" circuit identified in *Figure 8-3*. Please assume each gate has one unit gate delay irrespective of the type. Verify this using Micro-Logic.

3) Complete the following table of expected operation for obtaining the sum of X=01110 and Y=00101. Note that the numbers are applied least significant bit first and the initial value of C is "0".
4) Use Micro-Logic to simulate the serial adder. Have printouts of the circuit, pattern file, timing diagram, and vector output.

Table of Expected Operation:

	t1	t2	t3	t4	t5
X	0	1	1	1	0
Y	1	0	1	0	0
C	(0)	(0)	(0)	( )	( )
CO	0	0	( )	( )	( )
S	1	1	( )	( )	( )

Procedure:

1) Construct the circuit using switch #1 for X, switch #2 for Y and the momentary switch for the clock. Connect switch #3 to the clear line. Connect C, CO and S to LEDs 2, 3 and 4 respectively.
2) Clear the serial adder (i.e. set the D latch to "0").
3) Set X and Y to the specified values. Verify and record the values for CO and S.
4) Press the momentary switch which generates an active high pulse of a duration of approximately 10 milliseconds.
5) Verify and record the correct value for C for the next operation. It should be the same as the previous CO.
6) Repeat steps 3 to 5.

Questions:

(To be incorporated within the Conclusion section of your lab report.)

- What would happen to the serial adder if the clear was kept on "0"?
- What was the propagation delay of your design for Experiment #4 (3-Bit Adder)? Assume that each gate is 1 unit gate delay.
- Compare the parallel adder to a serial adder which has a clock repetition rate of 10 gate delays and adds 3-bit binary numbers. Will the serial ever be faster than the parallel? If yes, explain.
- Assign a weight to 1 for each "gate". Perform an analysis similar to the above for the difference in hardware. For what value of n (where is n is the number of bits) will the serial adder be more space or gate efficient?